9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 – REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High Impedance
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

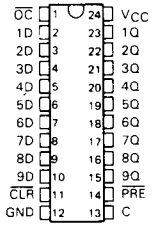
The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

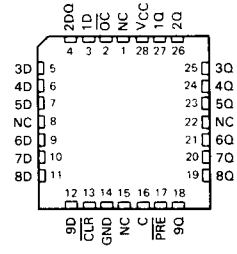
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS843 and SN74ALS844 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS843 and SN54ALS844.

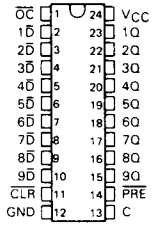
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . DW OR NT PACKAGE
(TOP VIEW)



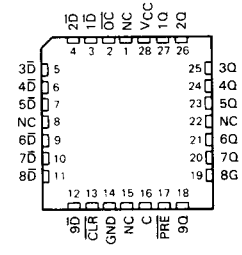
SN54ALS843, SN54AS843. . . FK PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . FK PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE
(TOP VIEW)



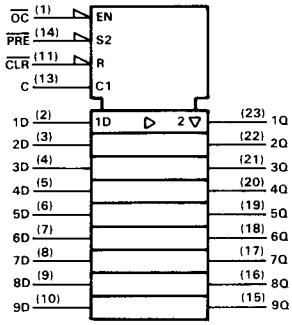
NC – No internal connection

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C.

'ALS843, 'AS843 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_O
X	X	H	X	X	Z

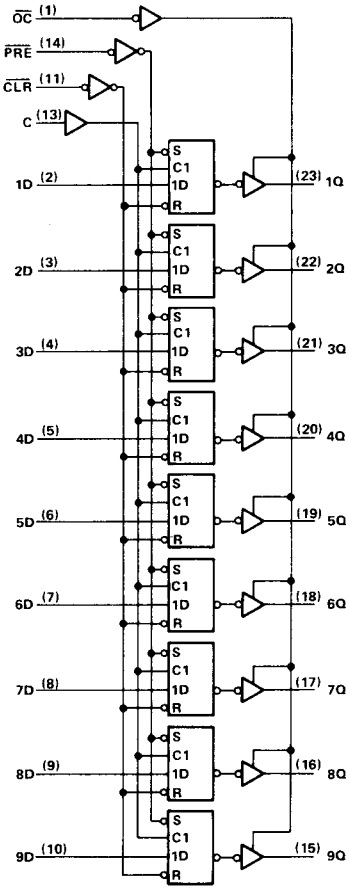
'ALS843, 'AS843 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS843, 'AS843 logic diagram (positive logic)



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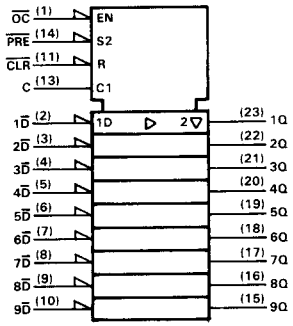
'ALS844, 'AS844 FUNCTION TABLE

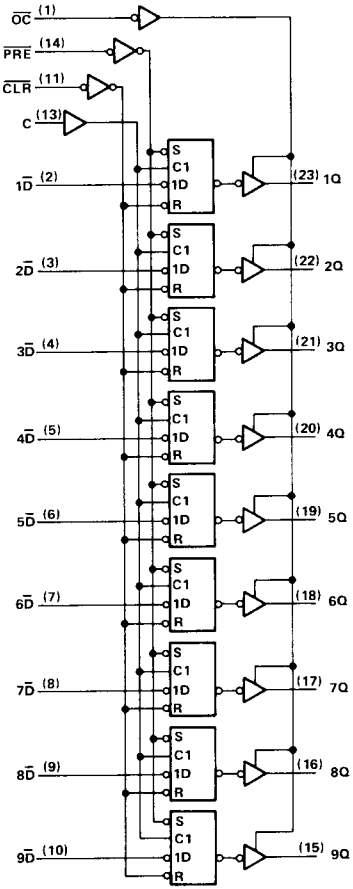
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_O
X	X	H	X	X	Z

'ALS844, 'AS844 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

'ALS844, 'AS844 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0. 7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (−1 versions)					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS843	V_{CC} = 5.5 V	Outputs high		21	36		21	36	mA
			Outputs low		41	67		41	67	
			Outputs disabled		25	42		25	42	
	'ALS844		Outputs high		21	36		21	36	
			Outputs low		41	72		41	72	
			Outputs disabled		28	48		28	48	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS843			SN54ALS843		SN74ALS843		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	15	2	13	ns
t_{PHL}				11	15	4	20	4	18	
t_{PLH}	C	Q		12	18	5	25	5	21	ns
t_{PHL}				16	23	8	30	8	26	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	5	22	ns
t_{PHL}				19	26	4	35	6	30	
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				14	21	6	27	6	23	
t_{PZH}	$\overline{OC}$	Q		7	10	2	14	2	12	ns
t_{PZL}				9	12	4	16	4	14	
t_{PHZ}	$\overline{OC}$	Q		6	9	2	12	2	10	ns
t_{PLZ}				7	10	2	14	2	12	

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS844			SN54ALS844		SN74ALS844		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q		11	16	4	22	4	20	ns
t_{PHL}				9	13	3	17	3	15	
t_{PLH}	C	Q		17	24	8	32	8	29	ns
t_{PHL}				14	19	6	26	6	22	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	5	22	ns
t_{PHL}				19	26	4	35	6	30	
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				16	23	8	29	8	25	
t_{PZH}	$\overline{OC}$	Q		10	15	2	19	4	17	ns
t_{PZL}				12	18	3	22	5	20	
t_{PHZ}	$\overline{OC}$	Q		7	10	1	12	1	11	ns
t_{PLZ}				5	9	1	14	1	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration, enable C high	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS843	V_{CC} = 5.5 V,	Outputs high		37	62		37	62	mA
			Outputs low		56	92		56	92	
			Outputs disabled		56	92		56	92	
	'AS844		Outputs high		39	64		39	64	
			Outputs low		58	95		58	95	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.